A HIGH PERFORMANCE COMMAND AND DATA HANDLING SYSTEM FOR NASA'S LUNAR RECONNAISSANCE ORBITER

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A high performance, modular and state-of-the-art Command and Data Handling (C&DH) system has been developed for use on the Lunar Reconnaissance Orbiter (LRO) mission. This paper addresses the hardware architecture, the operational performance, and the fabrication technology.

I. Introduction

LRO is the first mission in NASA's Vision for Space Exploration which is a plan to return to the moon and then to travel to Mars and beyond. LRO will launch in early 2009 with several key objectives: to find safe landing sites, locate potential resources, characterize the radiation environment, and demonstrate new technology. LRO will spend at least a year mapping the surface of the moon. Data from the orbiter will help NASA select safe landing sites for astronauts, identify lunar resources and study how the moon's environment will affect humans[1].

The C&DH was developed by NASA's Goddard Space Flight Center and is the heart of the LRO avionics. It is designed to support uplink command processing and execution, telemetry generation, guidance and control algorithms, provide interfaces to all of the avionics data interfaces, and collect science data from the instruments. It also provides autonomous failure detection and handling capabilities including a low level watchdog hierarchy, provides the spacecraft with a timing pulse, and provides data storage of 384 Gigabits between telemetry passes. The C&DH has been successfully environmentally tested and delivered to the LRO spacecraft for the flight Integration and Test.

The LRO C&DH design is also used on the Lunar Crater Observation and Sensing Satellite (LCROSS). LCROSS is managed by NASA Ames Research Center and will travel to the Moon as a co-manifested payload aboard the Atlas 5 launch vehicle along with LRO[2]. In addition, several key elements of the LRO C&DH design are baselined for future NASA missions such as Global Precipitation Measurement (GPM) and Magnetospheric MultiScale (MMS).

The LRO spacecraft architecture utilizes reliable standard data buses for data transfers and control. A SpaceWire network is used for high speed data transfers and a MIL-STD-1553 bus for lower data rate transfers. This versatile system allows the C&DH to incorporate a hybrid implementation in which the SpaceWire network, the 1553 bus, legacy serial data connections, and a PCI bus are all utilized to interconnect the C&DH with the spacecraft subsystems and instruments. LRO will be the first mission in space to use the full network capability of SpaceWire.

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II. C&DH System Overview

The implementation of the LRO C&DH is based on a cost and schedule driven approach, capitalizing on strong in-house heritage designs and expertise. The system architecture is designed to utilize standardization, small physical size, low-power, high-performance capability and high reliability for space applications. To achieve the LRO mission success criteria, three areas important to the C&DH design were identified. These areas are (1) telemetry generation and command processing, (2) collection of science data from instruments, (3) and storage of science and housekeeping data between telemetry downlink passes. These areas have been extensively architected and implemented.

III. C&DH FEATURES

The C&DH team capitalized on extensive experience with hardware and software with PCI bus design, SpaceWire networking, Actel FPGA design, digital flight design techniques, and the use of VxWorks for the real-time operating system. The resulting hardware architecture depicted in Figure 1 was implemented to meet the LRO mission requirements.

In addition, the use of industry standard interfaces (SpaceWire, 1553, PCI, RS-422) allows access to relatively inexpensive and commercially available data simulators for ground support equipment. Intellectual Property (IP) was also available commercially for the cores for the digital designs. Several IP items were developed at Goddard and were used in the C&DH design of various Actel field programmable gate arrays (FPGA), specifically the Four-Port SpaceWire Router Core and the PCI interface core. Digital logic was designed to maximize the use of the Actel radiation-tolerant RTAX-2000 FPGA as much as possible.

A. Telemetry and Command

LRO utilizes two radio frequency (RF) bands for its communications with Earth. The S-Band is used for command and telemetry of housekeeping data. The Ka-Band is used for high speed data transfer of science data. To accommodate this, the C&DH utilizes two similar designs on a single assembly, with each design dedicated to a single band.

B. Collection of Science Data

The extensive use of SpaceWire European Cooperation for Space Standardization (ECSS-E-50-12A) and MIL-STD-1553 allows for expandability and scalability. Late addition of additional nodes can be accommodated anywhere in the spacecraft and attached to the C&DH SpaceWire network seamlessly.

The C&DH provides a mission unique interface to the LAMP instrument as well as providing timing synchronization to all the instruments.

C. Data Storage

The C&DH provides a mass storage system for the LRO spacecraft with a storage capacity of 48 Gigabytes (GB). Data collected from the instruments and the avionics housekeeping data is kept within this storage system prior to playback during a telemetry pass.

D. System Architecture

Figure 1 depicts the C&DH Subsystem with its ten sub-assemblies. The figure illustrates a top-level block diagram of the C&DH with the LRO Avionics and instrument interfaces. It also shows the interconnections between the C&DH sub-assemblies and other subsystems: the Ka-Band transmitter, S-Band transponder, and seven LRO instruments.

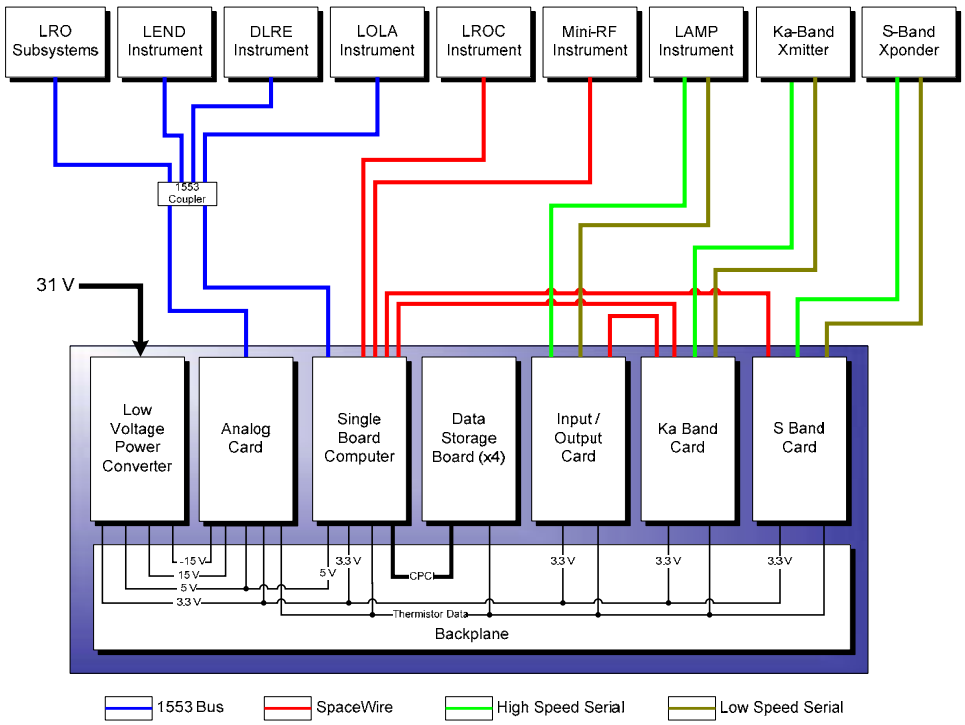

Figure 1. C&DH Architecture.

IV. C&DH SUB-ASSEMBLIES

The C&DH is comprised of an enclosure, a backplane, a low voltage power converter, a single board computer, a communications interface board, four data storage boards, a housekeeping and digital input/output board, and an analog data acquisition board. These components are all contained within the same C&DH enclosure. All electrical connections between these components are made via the backplane for internal power distribution and PCI bus data transfers. The interfaces between the C&DH and the instruments and avionics are connected through a SpaceWire network, a MIL-STD-1553 bus, and a combination of synchronous and asynchronous serial data transfers over RS-422 and LVDS electrical interfaces. The C&DH acts as the spacecraft data system with an instrument data manager providing all software and internal bus scheduling, ingestion of science data, distribution of commands, and performing science operations in real-time.

Figure 2 shows the fabricated engineering test unit versions of the sub-assemblies. Seven of the sub-assemblies were designed at GSFC. Only the single board computer (SBC) was procured commercially.

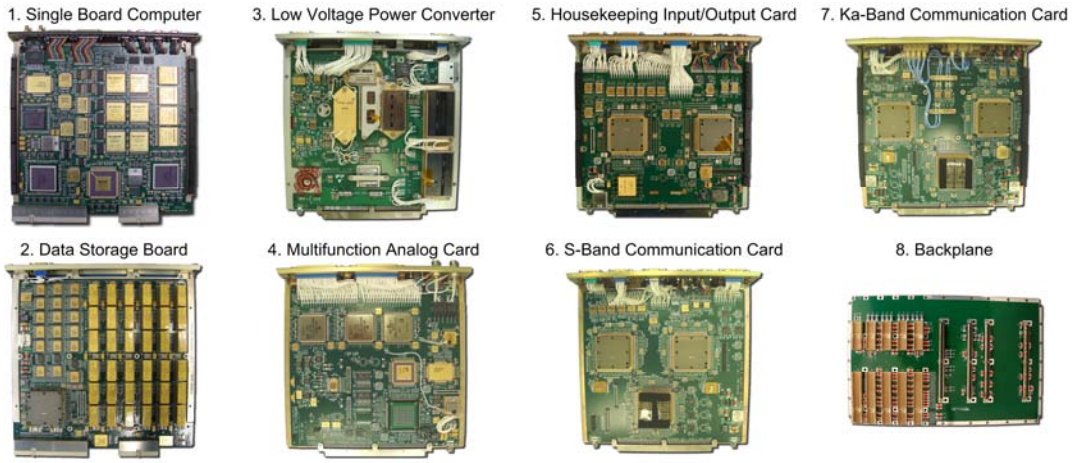

Figure 2. C&DH Sub-assemblies.

A. Single Board Computer

The SBC is the processing platform for the flight software (FSW) and the attitude control software (ACS). The SBC utilizes the RAD750 processor, operating at a frequency of 133 Megahertz (MHz). The SBC is designed to be immune to latchup and sustain up to 50 Krads of total ionizing dose. For memory, the SBC contains 36 megabytes of (MB) of Static Random Access Memory (SRAM) for storing executable code and housekeeping data, 64 kilobytes of Start Up Read Only Memory (SUROM) for storing essential bootstrap code, and 4 MB of Electrically Erasable Programmable Read Only Memory (EEPROM) for storing application code. The EEPROM is arranged as two banks to store two copies of the application code. The SBC operates as the bus controller for the 1553B bus to communicate with LRO subsystems and the instruments. Four SpaceWire interfaces are provided and are used to communicate with the LROC and Mini-RF instruments and both communication cards (S-Band and Ka-Band). The backplane connector provides a compact PCI bus interface which is utilized to transfer data with all four data storage boards.

B. Housekeeping Input/Output Board

The HKIO is a mission unique board and provides three functions within the C&DH: distribution of the 1 pulse per second (PPS) signal to LRO, maintain a mission elapsed timer (MET), and to provide an interface for the LAMP instrument.

The 1 PPS signal is generated within the HKIO by using a 20 MHz clock from one of the two ultra stable oscillators (USO). The MET is used to maintain the time of received uplink commands and as a mechanism for time synchronization.

Two interfaces are provided to the LAMP science instrument. Because LAMP is derived from an earlier instrument used on the New Horizons mission to Pluto (ALICE), the LAMP instrument's interface was not altered to reduce schedule risk and cost to LRO. The HKIO provides electrical and data connectivity to the LAMP instrument through two serial interfaces, one high speed interface using low voltage differential signaling (LVDS) and one low speed interface using the RS-422 standard. The science data and commands to and from the LAMP instrument go through the HKIO board and flows to the SBC using a SpaceWire link.

C. Multi-Function Analog Card

The MAC provides all analog connectivity for the C&DH for its internal telemetry for voltage monitoring and internal thermistors in addition to all the analog data from the LRO spacecraft. The analog data from the LRO spacecraft includes all thermistors, platinum resistance thermometers, hinge potentiometers, coarse sun sensors, various analog telemetry points, and pressure transducers. The MAC digitizes all the analog data and generates telemetry and receives commands over the 1553 bus.

In addition to providing analog telemetry values, the MAC also provides five switched power services. The services provide the spacecraft bus voltage to various heaters located near the LROC instrument and are controlled by flight software.

D. Data Storage Boards

The four DSBs are designed to be part of a file system which handles the storage and retrieval of files. The DSBs provide 384 gigabits at Beginning of Life (BOL) of memory capacity for storing science and housekeeping data during a 17.5 hour time interval between Ka-Band downlink passes. The file system mechanisms are supported by the SBC using the FAT32 file system.

The DSB contain error detection and correction (EDAC) logic circuitry to correct up to 2 nibbles (4 bits per nibble for a total of 8 bits) in error and to detecting three or more nibbles in error. The EDAC is implemented using a form of short Reed Solomon coding. In addition to the EDAC, the DSB provides a hardware based scrubber which will go through all the memory locations and clear out any bit errors. The scrubber is designed to be completely autonomous and does not need additional software support.

The DSBs utilizes synchronous dynamic random access memory (SDRAM) packaged in flight qualified high density memory modules as the memory storage element. The DSB can turn off all SDRAMs on a single board to conserve power when needed. All data transfers and configuration of the DSBs take place using the compact PCI interface through the backplane connector.

E. Ka-Band Communications Card

The Ka-Comm card provides high-speed telemetry to Earth using Ka-Band frequencies. For LRO, the Ka-Comm card is connected to the SBC via a SpaceWire link. During a Ka-Band pass, the data from the SBC flows directly into the Ka-Comm card at the SpaceWire link rate of 132 megabits per second (Mbps). The telemetry data rate itself

is 100 Mbps. Once the data is received by the Ka-Comm card from the SBC, the Ka-Comm card then proceeds to encode the data for transmission. The encoding is done as per Consultative Committee for Space Data Systems (CCSDS) recommendations for telemetry encoding. The Ka-Comm card also splits the telemetry stream into two streams for offset quadrature phase shift keying (OQPSK) modulation. The two streams are sent to the Ka-Band transmitter, which in turn modulates the data onto a radio-frequency (RF) carrier and is finally transmitted through the high gain antenna (HGA).

In addition to providing telemetry to the Ka-Band transmitter, the Ka-Comm card also provides command and control and receives housekeeping telemetry from the Ka-Band transmitter itself. This is accomplished by using an asynchronous low rate serial interface with RS-422.

F. S-Band Communications Card

The S-Comm card provides telemetry and receive commands to and from Earth using S-Band frequencies. For LRO, the S-Comm card is connected directly to the SBC via a SpaceWire link. During a pass, the data from the SBC flows directly into the S-Comm card at the SpaceWire link rate of 10 Mbps, where the telemetry data rate is a maximum 1 Mbps.

Once the data is received by the S-Comm card from the SBC, the S-Comm card then proceeds to encode the data for transmission. The encoding is done as per CCSDS recommendations for telemetry encoding. The S-Comm card provides a single data stream for Bi-Phase Shift Keying (BPSK) modulation in the S-Band transmitter. The data stream is sent to the S-Band transponder, at various data rates up to 1.093 Mbps (2.186 Mbps symbol rate), which is in turn modulated onto a RF carrier and transmitted through the HGA or omni-directional antennas.

For commands, S-Comm card accepts CCSDS telecommands from the S-Band transponder at various rates up to 4 kilobits per second (Kbps). The S-Comm card also generates a timing pulse upon receipt of command for time correlation with the ground stations.

The S-Comm card also provides command and control and receives housekeeping telemetry from the S-Band transponder itself. This is accomplished by using an asynchronous low rate serial interface over RS-422.

Finally, the S-Comm card provides the ability to process hardware decoded commands and are executed directly by the S-Comm card itself. Up to eight hardware-decoded commands are provided, four of which are RS-422 outputs and four are low voltage TTL.

G. Low Voltage Power Converter

The Low Voltage Power Converter (LVPC) is required to convert an input voltage with an operational range of +21 volts DC to +35 volts DC from the LRO spacecraft to provide voltage outputs of +3.3 VDC, +5 VDC and +/-15 VDC with EMI filtering. The LVPC also contains circuitry that drives the magnetic relays which provide power for several components of LRO's RF system. These RF components include the S-Band antenna transfer switch and the Ka-Band Traveling Wave Tube Amplifier (TWTA) power relay.

H. Backplane

The backplane provides interconnectivity for the nine cards in the LRO C&DH System within the confines of the C&DH enclosure. These cards include the S-Band and Ka-Band communication cards, the HK/IO card, the MAC, the LVPC, the SBC, and four DSB cards. The backplane accommodates each card that connects to it with a unique interface. The backplane distributes the voltage outputs from the LVPC. The backplane provides +5 VDC to the SBC and the MAC. In addition, +3.3 VDC is provided to all of the boards within the C&DH enclosure and +15 VDC to the MAC and the DSBs, and -15 VDC to the MAC.

The backplane also provides a compact PCI bus interface between the SBC and the four DSBs and is rated for 33 MHz data transfers. Thermistor data from all the boards is also provided and distributed through the backplane to the MAC as part of the housekeeping data collection.

I. Enclosure

The C&DH enclosure (Figure 3) acts as the mechanical housing for the C&DH unit and contains all of the C&DH hardware assemblies. The C&DH is 16.00 in (L) by 11.50 in (W) by 9.75 in (H) in dimensions and weighs 46 pounds with all its subassemblies installed. The C&DH box is mounted on the iso-thermal panel (ITP) of LRO's avionics deck. The flange at the base of the C&DH

Figure 3. C&DH Enclosure.

enclosure is used to attach the C&DH to the LRO structure with twenty (20) fasteners.

IV. SYSTEM OPERATIONAL PERFORMANCE

The flight C&DH unit for the LRO mission has successfully completed box-level environmental testing and comprehensive testing at the spacecraft level for hundreds of hours of spacecraft operation. The following sections highlight several significant operational performance metrics during the LRO integration and test (I & T) phase.

A. Spacecraft Autonomy

The baseline on-orbit LRO ground contact plan is four Ka-band downlink passes per day (duration of 45 minutes each) and twelve S-Band downlinks/uplinks contacts (duration of at least 30 minutes each) per day. Between the ground contacts, the flight software hosted by the C&DH provides autonomous operation of the spacecraft by issuing preplanned commands uploaded by ground into the processor's stored command memory. The flight software monitors the spacecraft house-keeping data for anomalies and responds to them with appropriate actions. Under worst case conditions, the spacecraft is designed so that it is able to miss ground contacts for periods of up to 28 hours and will be capable of sustaining itself without disrupting normal operations.

B. Processor Utilization and Power Dissipation

The C&DH is required to maintain less than 80% processor utilization under worst case conditions. The C&DH processor utilization is measured to be an average slightly less than 80% while a Ka-Band pass is active at 100 Mbps in addition to performing normal operational functions and collecting and processing science data. In this configuration, the C&DH consumed a steady state power draw of 95 Watts.

C. Watchdog Strategy

LRO utilizes a single string design architecture except where safety and reliability concerns require additional protection. As a result, the C&DH is built with minimal hardware redundancy. To mitigate the risk associated with a single string design, the watchdog strategy for the C&DH is implemented in both hardware and software. Several layers of protection are provided to handle processor faults and memory anomalies caused by software and/or hardware errors, including Single Event Upset (SEU) and latchup. The watchdog strategy utilizes a layered hierarchy that provides increasing levels of intervention and protection. The first layer is a software based watchdog in the flight software, followed by a second layer software based watchdog on the SBC. The last layer is the hardware watchdog on the S-Comm Card which recycles the power to the C&DH by issuing a command the LVPC as a last resort. This watchdog strategy for fault detection and correction has been successfully tested throughout integration and testing.

D. Science Data Collection

Data from all the science instruments is collected into files in the C&DH's data storage system. These files are constantly created while LRO orbits the moon. The science data is downlinked as much as possible during the Ka-Band passes by using the CCSDS file delivery protocol (CFDP). The use of the CFDP ensures that the science data is transferred in its entirety and error free before it is removed from the data storage system to free up space for new science data.

E. Ultra Stable Oscillators

The C&DH supports two Ultra Stable Oscillators (USO). One is designated as primary and the other as redundant. Only one of the oscillators is powered at any given time. Each oscillator provides two 20 MHz clock signals. One signal goes to the C&DH HKIO card for 1 PPS generation, and the second signal goes directly to the LOLA instrument.

The primary USO was chosen to meet a frequency stability factor of 10 parts per billion (ppb) over one millisecond (ms). The redundant USO was chosen to meet a frequency stability factor of 0.3 parts per million (ppm) over one millisecond (ms). The oscillators were chosen to provide sufficient stability to meet the needs of the laser ranging system component of the LOLA instrument.

V. FABRICATION TECHNOLOGY APPROACH

Due to the complexity of the design and a large amount of components needed to implement the design, the selection of the fabrication process was a challenge to the design team. To meet LRO requirements for weight and size, the C&DH was drastically reduced in weight and size during the design process compared to a system built

utilizing conventional fabrication methods. Three proven fabrication processes for spaceflight use were selected: the use of surface mount technology (SMT) components, ceramic column grid array (CCGA) packaging for semiconductor devices, and the use of two sided printed wiring board assemblies (PWA) with a heat sink core.

The following sections discuss these three processes in addition to addressing the vibration and thermal design problems.

A. Surface Mount Technology

Most of the C&DH subassemblies are populated with SMT components. A variety of SMT package styles such as flat-packs, quad flat-packs and leadless chip carrier (LCC) are utilized on the C&DH subassemblies. The use of SMT has two significant advantages, which are the small physical size of the components and the ability to use an automated assembly process. The use of automated assembly has helped to significantly improve the quality of the sub-assemblies by providing consistency throughout the assembly process. However, for space flight use, even SMT manufacturing processes must pass crucial thermal cycling qualification based on the mission environment profile. SMT components must withstand hundreds of thermal cycles over the mission's design life.

B. Ceramic Column Grid Array Design

CCGA array packaging was selected for the field programmable gate array device (FPGA) on the DSB. This packaging technology provided a sufficient number of input/output (I/O) pins for the DSB design in addition to providing a considerably smaller footprint with a comparable FPGA utilizing the ceramic quad flat-pack (CQFP) packaging.

The DSB is made more rigid by attaching a stiffening frame to the heatsink to meet the CCGA structural design criteria. For a CCGA device, the card deflection ratio must be sufficient with margin to ensure that the solder joints of the CCGA device do not fail. Figure 4 shows the structural analysis at 337 Hz to demonstrate that the board deflection is acceptable at the three sigma level.

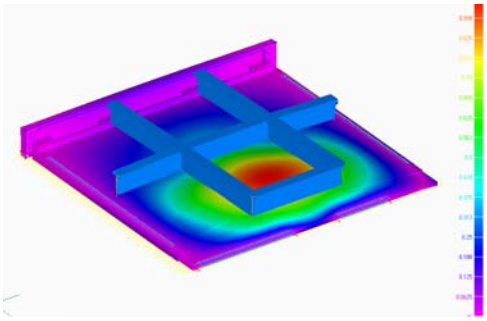

Figure 4. Structural analysis of DSB first mode with simple fixity at 337 Hz.

C. Two-Sided Printed Wiring Board Assembly

Each C&DH sub-assembly consists of a double-sided or single-sided printed wiring board (up to 12 layers 6U-160 mm), a heat sink plate, two wedge locks, an edge connector, a stiffener and a front panel. The aluminum heat sink is sandwiched between the two PWBs. The wedge locks are mounted on both long edges of the heat sink. For the DSBs and the SBC, the assembly is electrically and physically connected to the backplane through a HyperTronic cPCI connector. The remaining boards (HKIO, MAC, Ka-Comm, S-Comm) utilize a MEB 184-pin edge connector. A stiffener is attached to the heatsink to reduce the board deflection and dynamic stresses due to vibration.

Electrical connections between two PWBs on the same assembly are provided by z-wires. The use of z-wires is minimized where possible to improve the reliability of the overall assembly. The solder joint of the z-wire is also thoroughly inspected during manufacturing. The use of z-wires can reduce the overall signal length by providing a more direct path between two connection points. Signal integrity analysis was used to optimize the layout process.

A finite element analysis (FEA) was performed to help determine a suitable fabrication technique to mount the SDRAM packages onto the DSB assembly. The FEA showed that the stresses on the corners of the SDRAM devices required the addition of an epoxy to bring down the stress levels to within allowable limits for vibration levels.

D. Signal Integrity

Due to the use of high speed signals with fast edge rates, signal integrity (SI) analysis was performed on all of the digital PWB designs of the C&DH. The prevalence of the high speed digital logic elements necessitated an analysis of all the signal interconnects for all the boards to ensure that the signals were within specifications with regard to monotonicity, overshoot, and undershoot. The signal integrity analysis was performed during the board layout and signal routing phases to determine whether signals needed to be terminated to address signal integrity. The analysis ensured that all digital signals were within the component's electrical specification. In addition to signal quality, the effects of crosstalk on all signals were analyzed and mitigated where possible.

E. Thermal Design

The C&DH is designed for an operating temperature range of -10 to +40 C and a survival temperature range of -20 to +50 C. The qualification test base plate temperature for the LRO C&DH was performed from -20 to +50 C. The thermal analysis models for the chassis and board shown in figures 5 and 6 are based on conducted cooling through the base plate to the spacecraft mounting surface controlled to a constant 50 C. The main thermal paths of the modules are through the top and bottom wedge lock interfaces at the thermal steady state condition.

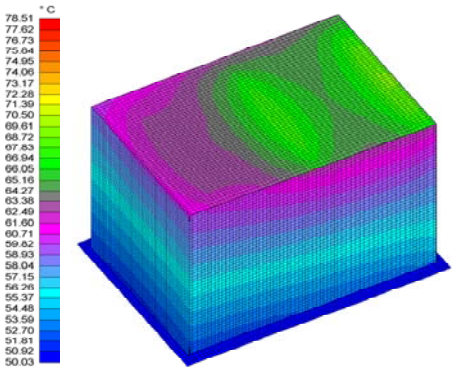

Figure 5. C&DH Thermal Profile.

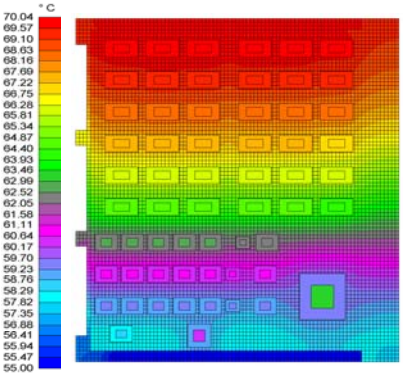

Figure 6. DSB Thermal Profile.

VI. CONCLUSIONS

The C&DH hardware and software performed well throughout the LRO integration and test phases. The C&DH is relatively small in size and light in weight, but it is capable of performing several sophisticated tasks.

The underlying philosophy utilized by the design team was to guarantee the design by simulation (for both digital designs and signal integrity) as much as possible. The testing of the completed sub-assemblies was intended to validate the design. This design approach reduced the risk of surprise of design errors and inadequacies.

The C&DH utilizes a versatile architecture and industry standards to provide high performance in a small reliable package. The C&DH is a spacecraft data system with the capability to collect science data from the instruments and store it in its data storage system for the LRO mission. Due to its flexibility and modularity, it can be reused on other NASA missions with similar requirements and architecture.

REFERENCES

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